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# Temperature dependent characterization of gallium arsenide X-ray mesa p-i-n photodiodes

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Electrical characterization of two GaAs p<sup>+</sup>-i-n<sup>+</sup> mesa X-ray photodiodes over the temperature range 0 °C to 120 °C together with characterization of one of the diodes as an X-ray detector over the temperature range 0 °C to 60 °C is reported as part of the development of photon counting X-ray spectroscopic systems for harsh environments. The randomly selected diodes were fully etched and unpassivated. The diodes were 200 μm in diameter and had 7 μm thick i layers. The leakage current density was found to increase from  $(3 \pm 1) \text{ nA/cm}^{-2}$  at 0 °C to  $(24.36 \pm 0.05) \mu\text{A/cm}^{-2}$  at 120 °C for D1 and from a current density smaller than the uncertainty  $(0.2 \pm 1.2) \text{ nA/cm}^{-2}$  at 0 °C to  $(9.39 \pm 0.02) \mu\text{A/cm}^{-2}$  at 120 °C for D2 at the maximum investigated reverse bias (15 V). The best energy resolution (*FWHM* at 5.9 keV) was achieved at 5 V reverse bias, at each temperature; 730 eV at 0 °C, 750 eV at 20 °C, 770 eV at 40 °C, and 840 eV at 60 °C. It was found that the parallel white noise was the main source of the photopeak broadening only when the detector operated at 60 °C, at 5 V, 10 V, and 15 V reverse bias and at long shaping times ( $>5 \mu\text{s}$ ), whereas the sum of the dielectric noise and charge trapping noise was the dominant source of noise for all the other spectra. © 2016 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4944892>]

## I. INTRODUCTION

Gallium arsenide is a semiconductor material of great interest for its use in photon counting X-ray spectroscopic detector systems. Its relatively wide bandgap ( $=1.42 \text{ eV}$  (Ref. 1)) compared to materials, such as Si and Ge, results in lower leakage current densities which allow X-ray detection at room and elevated temperatures.<sup>2</sup> Furthermore, its relatively low electron-hole pair creation energy ( $=4.184 \text{ eV}$  (Ref. 1)) allows similar statistics and spectroscopic resolution to Si. Another advantage of GaAs is its effective atomic number which provides high detection efficiency per unit thickness. Additionally, GaAs has been demonstrated to be more radiation resistant than Si for  $\gamma$ -rays,<sup>3,4</sup> electrons,<sup>5</sup> and low energy hadrons.<sup>6</sup> Consequently, the use of GaAs detectors can eliminate the need for cooling systems and radiation shielding when operating at harsh environments. Applications which may benefit from the use of GaAs detectors include space missions and terrestrial applications outside the laboratory environment which have restrictions on mass, power, and volume. Extreme environments can be experienced at X-ray fluorescence spectroscopy missions to Mercury and environments close to the sun (high temperatures<sup>7</sup>) and Jupiter (intense radiation<sup>8</sup>), as well as in engines and other oil lubricated machinery for real time X-ray fluorescence spectrometry condition monitoring.<sup>9</sup>

Due to its advantageous properties, GaAs has intensively been investigated for X-ray detection over the past years. A  $5 \times 5$  GaAs diode array structure was reported; its

ultrapure epitaxial planar layer, p<sup>+</sup>-i-n<sup>+</sup> structure, Schottky contact at the p<sup>+</sup> layer, and the guard ring all contributed to the low dark current densities ( $<6 \text{ nA/cm}^{-2}$  at room temperature).<sup>10</sup> An energy resolution (*FWHM*) of 0.266 keV at 5.9 keV at room temperature was reported with these devices, after coupling them to ultra low noise front end electronics.<sup>10</sup> Following this, larger devices with a thicker epilayer and similar structure to the detectors reported in Ref. 10 in a  $32 \times 32$  pixel array have been reported with an energy resolution of 0.3 keV *FWHM* at 5.9 keV at room temperature.<sup>11</sup> Research has also been conducted on GaAs p<sup>+</sup>-i-n<sup>+</sup> mesa X-ray photodiodes. High temperature (up to 90 °C) X-ray detection characterization of GaAs p<sup>+</sup>-i-n<sup>+</sup> diodes (2 μm thick i-layer) has been reported.<sup>12</sup> Furthermore, the X-ray detection of GaAs p<sup>+</sup>-i-n<sup>+</sup> diodes (3 μm thick i-layer) as a function of photon energy at 33.3 °C was studied.<sup>13</sup> A fabrication study of GaAs mesa photodiodes regarding the effects of the wet chemical etchants and etch depths on the dark currents has also been reported.<sup>14</sup>

Room temperature results characterising two randomly selected fully etched 200 μm GaAs p<sup>+</sup>-i-n<sup>+</sup> mesa X-ray photodiodes with 7 μm thick i-layers have been previously presented.<sup>15</sup> Here, we report the electrical characterization of the same diodes at the temperature range 0 °C to 120 °C, and we present X-ray spectra accumulated with one of the diodes operated in the temperature range 0 °C to 60 °C.

## II. DEVICE STRUCTURE

GaAs epilayers were grown on a 350 μm thick heavily doped, n<sup>+</sup> GaAs substrate by metal organic vapor deposition at the EPSRC National Centre for III-V Technologies,

<sup>a)</sup>Author to whom correspondence should be addressed. Electronic mail: G.Lioliou@sussex.ac.uk. Tel.: +44 (0) 1273 872568.

TABLE I. Layers structure of the GaAs  $p^+-i-n^+$  wafer.

Material	Type	Thickness (nm)	Doping density ( $\text{cm}^{-3}$ )
GaAs	$p^+$	10	$1 \times 10^{19}$
GaAs	$p^+$	500	$2 \times 10^{18}$
GaAs	i	7000	Undoped
GaAs	$n^+$	1000	$2 \times 10^{18}$
GaAs	$n^+$ (substrate)	...	...

Sheffield, UK. The thickness of the unintentionally doped i layer was  $7 \mu\text{m}$ , and it was grown between a  $1 \mu\text{m}$  n type and a  $0.5 \mu\text{m}$  p type GaAs layer. The p and n type dopants used were carbon and silicon, and the doping density of both n type and p type layers was  $2 \times 10^{18} \text{cm}^{-3}$ , as indicated by the supplier. Table I summarises the wafer's layer structure. Mesa diodes with diameters of  $200 \mu\text{m}$  were chemically etched using  $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  as the chemical etchant. The etched depth, as measured from the top of the wafer, was  $8.3 \mu\text{m}$ . The Ohmic contact of the active side, p side, was formed from Ti (20 nm thickness) and Au (200 nm thickness) layer.

### III. ELECTRICAL CHARACTERIZATION

#### A. Current measurements

The current as a function of applied forward and reverse bias of both diodes was measured using a Keithley 6487 Picoammeter/Voltage Source. The diodes were installed inside a TAS Micro MT climatic cabinet for temperature control. The temperature was initially set to  $120^\circ\text{C}$  and decreased to  $0^\circ\text{C}$ . The diodes were left to stabilize at each temperature for 30 min before the measurements were started. The measured dark current as a function of applied forward bias and temperature for both diodes D1 and D2 can be seen in Fig. 1.

For forward applied biases,  $V_F$ , the dark current decreased with decreased temperature. The forward current,  $I_F$ , can be defined by the recombination current,  $I_{FR}$ , whose temperature dependence is

$$I_{FR} \propto n_i \exp\left(\frac{qV_F}{2kT}\right), \quad (1)$$

and the diffusion current whose temperature dependence is

$$I_{FD} \propto n_i^2 \exp\left(\frac{qV_F}{kT}\right), \quad (2)$$

where  $n_i$  is the intrinsic carrier concentration of the semiconductor material at a given temperature  $T$ ,  $q$  is the charge of an electron, and  $k$  is the Boltzmann constant.<sup>16</sup> The data presented in Fig. 1 were found to be better described by Eq. (1) rather than Eq. (2) suggesting that the forward current was defined by the recombination current rather than the diffusion current. More specifically, the same proportionality factor was calculated using Eq. (1) over the investigated temperature range, for each forward bias and for each diode, unlike when using Eq. (2). The saturation current,  $I_0$ , and the ideality factor,  $n$ , were calculated for each device, at each temperature, based on the linear region of their semi-logarithm  $I$ - $V$  characteristics ( $V_F < 1 \text{ V}$ ) as described in Ref. 17

$$I_F = I_0 \exp\left(\frac{qV_F}{nkT}\right). \quad (3)$$

A line of best fit was calculated for the semi-logarithm current as a function of forward bias using linear least squares fitting. Equation (3) is valid when  $V_F > 3kT/q$ . The saturation current was found to vary from  $(4.4 \pm 0.7) \times 10^{-10} \text{ A}$  at  $120^\circ\text{C}$  to  $(4.0 \pm 0.2) \times 10^{-14} \text{ A}$  at  $0^\circ\text{C}$  for D1 and from  $(4 \pm 1) \times 10^{-10} \text{ A}$  at  $120^\circ\text{C}$  to  $(3.6 \pm 0.2) \times 10^{-14} \text{ A}$  at  $0^\circ\text{C}$  for D2. The calculated ideality factor as a function of temperature can be seen in Fig. 2.

The ideality factor improved from  $(1.94 \pm 0.01)$  at  $0^\circ\text{C}$  for both devices to  $(1.78 \pm 0.03)$  and  $(1.79 \pm 0.05)$  at  $120^\circ\text{C}$  for D1 and D2, respectively. Although the ideality factor was temperature dependent, the small decrease of  $n$  as the temperature increased was not sufficient to indicate significant contribution of tunnelling in the conduction process.<sup>17</sup> The semi-logarithm  $I$ - $V$  characteristics of the devices (Fig. 1) showed a non-linear region for  $V_F \geq 1 \text{ V}$  which originated from the effect of the series resistance.<sup>16</sup>

The leakage current,  $I_R$ , as a function of reverse applied bias of the two GaAs  $p^+-i-n^+$  mesa photodiodes is shown in Fig. 3. The leakage current was decreased with decreased temperature for all investigated reverse biases. More specifically, the leakage current of D1 at  $15 \text{ V}$  reverse bias decreased from  $(7.65 \pm 0.01) \times 10^{-9} \text{ A}$  at  $120^\circ\text{C}$  to  $(9 \pm 4) \times 10^{-13} \text{ A}$  at  $0^\circ\text{C}$ , whereas D2 showed lower dark current which decreased from  $(2.950 \pm 0.007) \times 10^{-9} \text{ A}$  at  $120^\circ\text{C}$  to a current smaller than the uncertainty of the measurement  $(0.8 \pm 4.0) \times 10^{-13} \text{ A}$  at  $0^\circ\text{C}$ , at the same applied reverse bias. The difference in the measured leakage current of the two devices was attributed to small variations arising from fabrication process and possibly variations in wafer

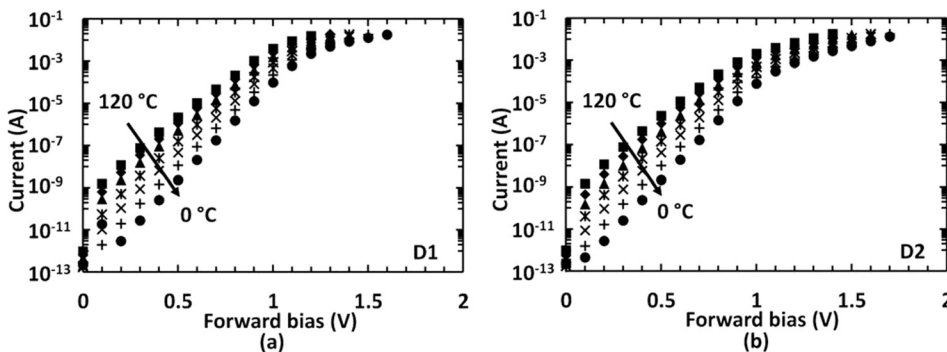


FIG. 1. Current as a function of applied forward bias for (a) D1 and (b) D2 in the temperature range  $0^\circ\text{C}$  to  $120^\circ\text{C}$ .



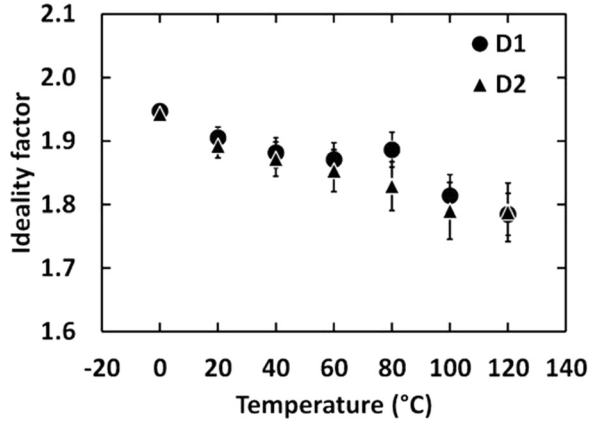


FIG. 2. Ideality factor extracted from the measured current as a function of applied forward bias for D1 (circles) and D2 (triangles) in the temperature range 0 °C to 120 °C.

quality. The leakage current density at 15 V reverse bias (21.4 kV/cm) of both devices as a function of temperature can be seen in Fig. 4. The leakage current density,  $J_R$ , of both devices showed an exponential decrease with a constant factor as the temperature decreased from 100 °C to 0 °C. However, Fig. 4 suggested that the leakage current mechanism at the temperature range 120 °C to 100 °C was different compared to lower temperatures.

The reverse current density,  $J_R$ , is given by

$$J_R = qn_i^2 \left( \frac{1}{N_d} \sqrt{\frac{D_p}{\tau_p}} + \frac{1}{N_a} \sqrt{\frac{D_n}{\tau_n}} \right) + q \frac{n_i}{2\tau_g} W, \quad (4)$$

where the first term is the diffusion current and the second term is the generation current.<sup>18</sup> In Eq. (4),  $N_d$  and  $N_a$  are the donor and acceptor impurity concentrations, respectively,  $D_p$  and  $D_n$  are the diffusion coefficient for holes and electrons, respectively,  $\tau_p$  and  $\tau_n$  are the carrier lifetime for holes and electrons, respectively,  $\tau_g$  is the carrier generation lifetime, and  $W$  is the depletion layer width. The diffusion current scales with  $n_i^2$  and the generation current scales with  $n_i$ . Since<sup>16</sup>

$$n_i^2 \propto \exp\left(-\frac{E_g}{kT}\right), \quad (5)$$

and

$$n_i \propto \exp\left(-\frac{E_g}{2kT}\right), \quad (6)$$

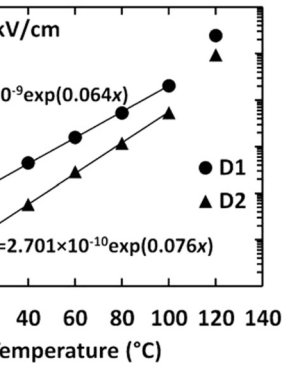
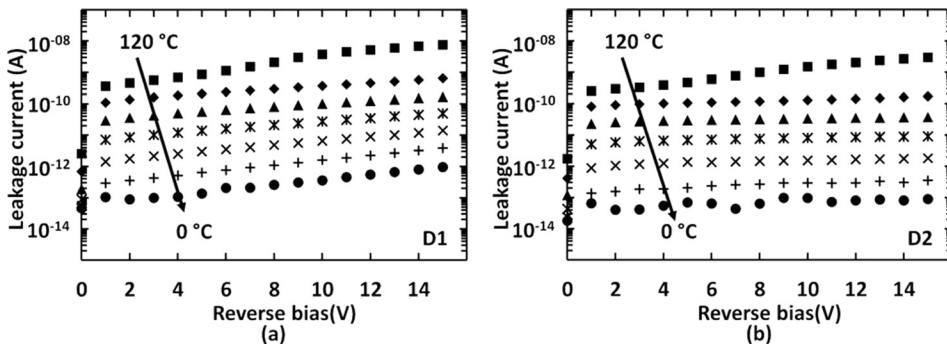


FIG. 4. Measured leakage current density as a function of temperature at 21.4 kV/cm internal electric field for D1 (circles) and D2 (triangles). The line of best fit at the temperature range 0 °C to 100 °C can also be seen.

a plot of  $\ln(J_R) - 1/kT$  should yield a straight line whose slope determines whether the generation or the diffusion current dominates. More specifically, a slope of approximately  $-E_g/2$  suggests that the dominant leakage current mechanism is generation, whereas a slope of approximately  $E_g$  suggests that the diffusion current dominates.<sup>18</sup> The  $\ln(J_R) - 1/kT$  graph was plotted for diode D1 and can be seen in Fig. 5. Two linear regions can be seen in Fig. 5, where the lines of best fit were calculated using linear least squares fitting. The prevailing conduction process at the temperature range 0 °C to 100 °C was found to be generation given that the slope of the  $\ln(J_R) - 1/kT$  is approximately  $-E_g/2$ , and the diffusion current dominated for temperatures higher than 100 °C given that the slope of the  $\ln(J_R) - 1/kT$  is approximately  $-E_g$ .

Both GaAs p<sup>+</sup>-i-n<sup>+</sup> diodes showed comparable leakage current densities to other high quality GaAs p-i-n diodes at temperatures close to room temperature. More specifically, diode D1 had a leakage current density of  $(22.3 \pm 0.9)$  nA/cm<sup>2</sup> and D2 had a leakage current density of  $(2.6 \pm 0.1)$  nA/cm<sup>2</sup> at 30 °C and at 21.4 kV/cm internal electric field (calculated based on Fig. 4). Other high quality GaAs p-i-n diodes had a leakage current density of  $\sim 10$  nA/cm<sup>2</sup> at the same temperature and internal electric field.<sup>2</sup>

## B. Capacitance measurements

The depletion width and the doping concentration in the i layer were calculated for both devices as a function of temperature based on temperature dependence capacitance measurements at the temperature range 0 °C to 120 °C. The capacitance measurements were performed using an HP 4275A Multi

FIG. 3. Leakage current as a function of applied reverse bias for (a) D1 and (b) D2 in the temperature range 0 °C to 120 °C.

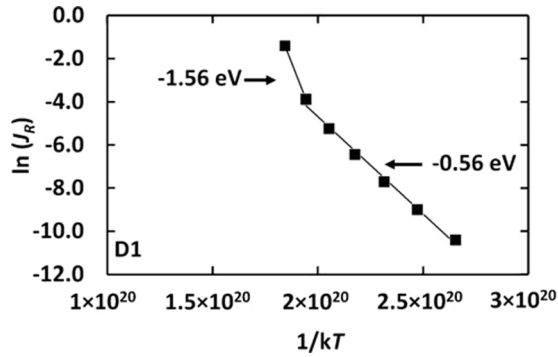


FIG. 5.  $\ln(I_R)$  as a function of  $1/kT$  for D1. The line of best fit at the temperature range  $0^\circ\text{C}$  to  $100^\circ\text{C}$  and  $100^\circ\text{C}$  to  $120^\circ\text{C}$  can also be seen.

Frequency LCR meter, with its test signal having a 50 mV rms magnitude and 1 MHz frequency. The capacitance of the empty packages,  $C_{\text{pack}}$ , which was measured to be 0.6 pF based on capacitance measurements on empty packages, was subtracted from the measured total capacitance. The resulting capacitance, the junction capacitance, as a function of applied forward bias at the temperature range  $0^\circ\text{C}$  to  $120^\circ\text{C}$  can be seen in Fig. 6.

As the temperature decreased from  $120^\circ\text{C}$  to  $0^\circ\text{C}$ , the capacitance of both devices decreased at each applied forward bias. There is a significant contribution of the diffusion capacitance,  $C_D(V_F)$ , to the junction capacitance at forward applied biases due to the rearrangement of the minority carrier density.<sup>16</sup> Bearing in mind that the diffusion capacitance is directly proportional to the forward current,  $I_F$ , the temperature dependency of the forward biased capacitance (Fig. 6) was explained based on the temperature dependency of the forward current shown in Fig. 1.

The measured capacitance as a function of temperature at different applied reverse biases (0 V, 1 V, 10 V, and 15 V) for both devices can be seen in Fig. 7. When reverse biased, the junction capacitance was mostly defined by the depletion layer capacitance,  $C_{DL}(V_R)$ , rather than the diffusion capacitance.<sup>16</sup> A temperature invariant depletion layer capacitance was measured for reverse biases  $V_R > 1$  V. However, a capacitance increase with temperature was recorded for low reverse biases  $V_R \leq 1$  V. In order to explain this capacitance variation with temperature, the depletion width was plotted as a function of applied reverse bias for diode D1 at  $0^\circ\text{C}$  and  $120^\circ\text{C}$ .

The depletion layer width of the diodes as a function of applied reverse voltage,  $W(V_R)$ , was computed using the measured depletion layer capacitance,  $C_{DL}(V_R)$ , where

$$C_{DL}(V_R) = \frac{\epsilon_0 \epsilon A}{W(V_R)}, \quad (7)$$

and  $\epsilon_0$  is the permittivity of free space,  $\epsilon$  is the dielectric constant of GaAs, and  $A$  is the area of the device.<sup>16</sup> The calculated depletion width as a function of applied reverse bias of diode D1 at  $0^\circ\text{C}$  and  $120^\circ\text{C}$  can be seen in Fig. 8. The depletion width increased with applied reverse bias at both the lowest and highest investigated temperature, as was expected. The depletion width was found to decrease from  $(5.8 \pm 0.3) \mu\text{m}$  at  $0^\circ\text{C}$  to  $(4.8 \pm 0.2) \mu\text{m}$  at  $120^\circ\text{C}$  when no bias was applied. However, it was found to be  $(7.5 \pm 0.5) \mu\text{m}$  for both temperatures at 15 V reverse bias. Considering that the doping concentrations of the  $p^+$  and  $n^+$  layers are high compared to the  $i$  layer, and the extension of the depletion region to the  $p^+$  and  $n^+$  sides is negligible, and hence, the  $i$  layer thickness of D1 was found to be  $(7.5 \pm 0.5) \mu\text{m}$ . Another important observation, based on Fig. 8, is that the diode D1 was fully depleted at 5 V reverse bias when the temperature was  $0^\circ\text{C}$ . Although the diode was almost fully depleted at 6 V, full depletion was achieved at 14 V, when the temperature was  $120^\circ\text{C}$ . This may be explained by the presence of a thin region around the depletion layer with unionized dopants at low temperatures, similarly to Ref. 19. These dopants were progressively ionized with temperature and limited the extension of the depletion layer preventing the diode to be fully depleted at low reverse biases. The ratio between the thickness of this region and the depletion layer was lower for high reverse biases compared to low reverse biases resulting in an invariant capacitance with temperature at high reverse biases.

The  $i$  layer thickness of diode D2 was found to be  $(6.7 \pm 0.4) \mu\text{m}$ . The uncertainties of the calculated depletion widths were related to the uncertainty in the capacitance measurements ( $\pm 0.03$  pF).

The relationship between the  $C^{-2}$  and applied voltage,  $V_a$ , was found to be linear at the bias range  $-0.4$  V to  $0.4$  V. A line of best fit was calculated for the  $C^{-2}(V_a)$  data for both diodes at all investigated temperatures. The value of the built-in voltage,  $V_{bi}$ , was extracted from the voltage axis intercept point.<sup>16</sup> The built-in voltage was found to be temperature dependent and to decrease with increasing temperature from  $(1.42 \pm 0.06)$  V at  $0^\circ\text{C}$  to  $(0.70 \pm 0.05)$  V at  $120^\circ\text{C}$ , for D1, and  $(1.42 \pm 0.05)$  V at  $0^\circ\text{C}$  to  $(0.79 \pm 0.06)$  V at  $120^\circ\text{C}$ , for D2. The built-in voltage is inversely proportional to the intrinsic carrier density,  $n_i$ , of the semiconductor material.<sup>16</sup> Also, the intrinsic carrier density is directly proportional to temperature. Hence, the built-in voltage was expected to decrease with

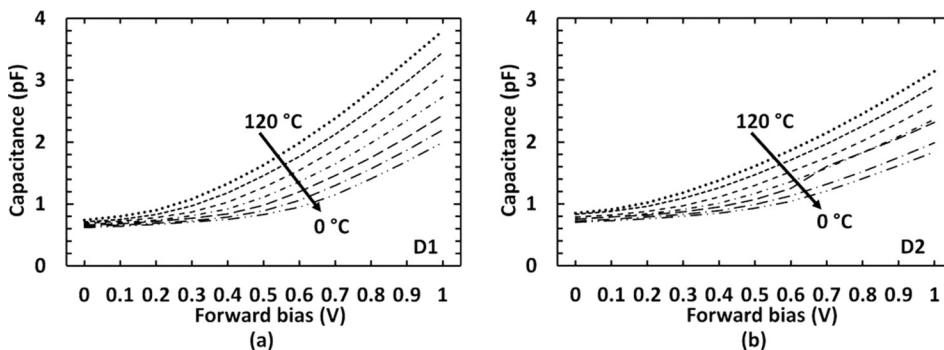


FIG. 6. Capacitance as a function of applied forward bias for (a) D1 and (b) D2 in the temperature range  $0^\circ\text{C}$  to  $120^\circ\text{C}$ .

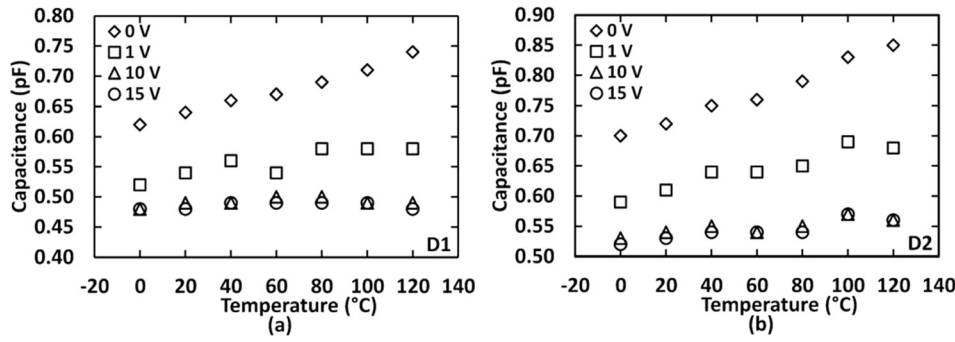


FIG. 7. Capacitance as a function of temperature for (a) D1 and (b) D2 in the range 0 °C to 120 °C at four reverse biases values.

increasing temperature, as it was also reported for a Si p-i-n diode in Ref. 17.

The carrier concentration of the i layer,  $N(W)$ , as a function of distance,  $W$ , below the  $p^+-i$  junction, based on the capacitance measurements of the junction,  $C_{DL}$ , when reverse biased was calculated using the equation for general nonuniform distributions<sup>16</sup>

$$\frac{d(1/C_{DL}^2)}{dV_R} = \frac{2}{q\epsilon_0\epsilon N(W)}, \quad (8)$$

and is shown in Fig. 9 for diode D1. It was found that the carrier concentration increased from  $(0.6 \pm 0.1) \times 10^{14} \text{ cm}^{-3}$  at 5  $\mu\text{m}$  below the  $p^+-i$  junction to  $(12.7 \pm 0.7) \times 10^{14} \text{ cm}^{-3}$  at the  $i-n^+$  interface for both temperatures. However, the doping profile of the i layer of D1 (Fig. 9) suggested that there might be a layer close to  $i-n^+$  junction with non-ionized dopants at 0 °C which were ionised at 120 °C. This is in accordance with the findings presented in Fig. 7, which show that the measured capacitance was temperature dependent in the temperature range 0 °C to 120 °C for low reverse biases  $V_R \leq 1 \text{ V}$ . The carrier concentration of D2 was found slightly higher than the carrier concentration of D1, varying from  $(0.87 \pm 0.02) \times 10^{14} \text{ cm}^{-3}$  at 5  $\mu\text{m}$  below the  $p^+-i$  junction to  $(16 \pm 9) \times 10^{14} \text{ cm}^{-3}$  at the  $i-n^+$  interface at 0 °C.

#### IV. X-RAY SPECTROSCOPY

X-ray spectra were obtained using the GaAs  $p^+-i-n^+$  photodiode D1 to characterize its X-ray detection performance as

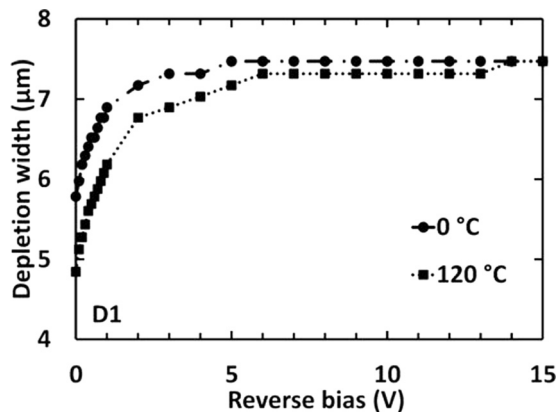


FIG. 8. Calculated depletion width for D1 calculated from capacitance measurements as a function of voltage at 0 °C and 120 °C.

a function of temperature. An  $^{55}\text{Fe}$  radioisotope X-ray source was positioned 3 mm above the top of the device. The diode was connected to a custom made, single channel, charge sensitive preamplifier without feedback resistor, similar to that reported in Ref. 20. The detector along with the preamplifier were installed inside a TAS Micro MT climatic cabinet throughout the measurements for temperature control. The signal of the preamplifier was shaped using an Ortec 572A shaping amplifier and was further connected to a multi-channel analyzer (MCA) for digitization.

The temperature was initially set to 60 °C and it was decreased to 0 °C with a 20 °C step. Spectra were accumulated at each temperature for different reverse bias conditions (0 V, 5 V, 10 V, and 15 V). The shaping time was varied, and spectra were obtained for  $\tau = 0.5 \mu\text{s}$ ,  $1 \mu\text{s}$ ,  $2 \mu\text{s}$ ,  $3 \mu\text{s}$ ,  $6 \mu\text{s}$ , and  $10 \mu\text{s}$  at each applied reverse bias. The live time of each spectrum was set to be 60 s. The accumulated spectra of the  $^{55}\text{Fe}$  radioisotope X-ray source at 0 °C and 60 °C with the best energy resolution (lowest  $FWHM$ ) can be seen in Fig. 10. The detected  $^{55}\text{Fe}$  photopeak is the combination of the characteristic Mn  $K\alpha$  (5.9 keV) and Mn  $K\beta$  (6.49 keV) lines of the  $^{55}\text{Fe}$  radioisotope X-ray source.<sup>21</sup> Gaussians were fitted to the peak taking into account the relative emission ratio<sup>21</sup> and the relative efficiency of the detector for the 5.9 keV and 6.49 keV peak. The spectra were energy calibrated based on the positions of the zero energy noise peak and the Mn  $K\alpha$  peak.

Possible partial charge collection of charge created in the non-active layers of the device resulted in the low energy tailing of the photopeak seen in Fig. 10, similarly to Ref. 22. The  $FWHM$  was measured for all obtained spectra. Figure 11 shows the  $FWHM$  of the 5.9 keV peak as measured at 5 V and 10 V reverse bias, as a function of temperature, for the

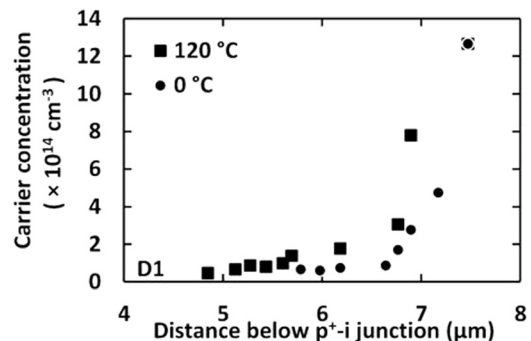


FIG. 9. Doping profiles of the i layer for D1 at 0 °C and 120 °C.

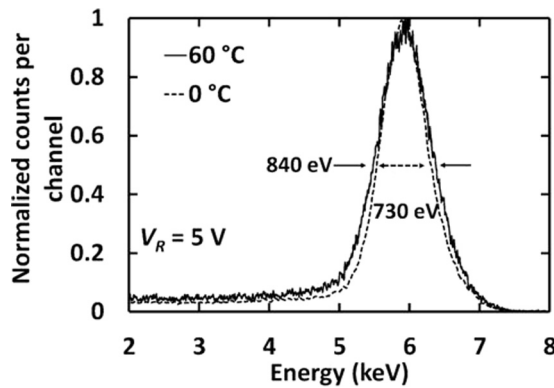


FIG. 10.  $^{55}\text{Fe}$  spectra accumulated with the GaAs  $p^+-i-n^+$  photodiode D1 at 5 V reverse bias at two different temperatures; 60 °C (solid line) and 0 °C (square dots).

optimum shaping time,  $\tau_{opt}$ . The  $FWHM$  increased as the temperature increased from 730 eV at 0 °C ( $\tau = 6 \mu\text{s}$ ) to 840 eV at 60 °C ( $\tau = 2 \mu\text{s}$ ) at 5 V reverse bias and from 740 eV at 0 °C ( $\tau = 10 \mu\text{s}$ ) to 910 eV at 60 °C ( $\tau = 2 \mu\text{s}$ ) at 10 V reverse bias. The noise of the system is analysed in Section V.

## V. NOISE ANALYSIS

The energy resolution of a non-avalanche semiconductor detector coupled to a charge sensitive preamplifier is degraded due to three independent sources of noise.<sup>23</sup> These are the Fano noise, due to the statistical nature of the X-ray absorption ionization process,<sup>24</sup> the charge trapping noise due to incomplete charge collection, and the electronics noise. The expected Fano limited resolution of the GaAs device at 5.9 keV was calculated to be 128 eV, assuming a Fano factor of 0.12<sup>25</sup> and an electron-hole pair creation energy of 4.184 eV.<sup>1</sup> Since the measured energy resolution is greater than the Fano noise, it can be said that there was a significant contribution from either the charge trapping noise or electronics noise.

The electronics noise, arising from the detector and the preamplifier, consists of the white parallel noise, white series noise,  $1/f$  noise, and dielectric noise. The first three noise sources were calculated as per Ref. 26, where a more detailed explanation of the noise components is given. The

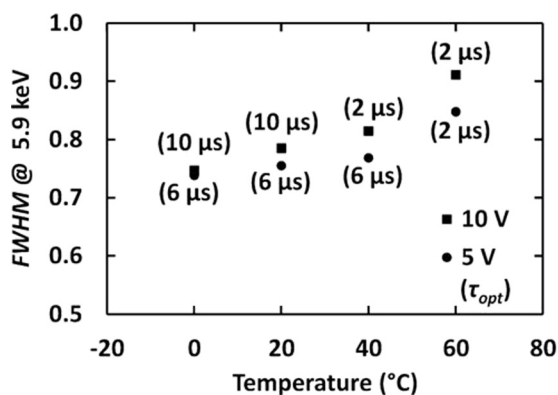


FIG. 11.  $FWHM$  of 5.9 keV peak as a function of temperature at 5 V (circles) and 10 V (squares) reverse bias, at the optimum shaping time.

white parallel noise, due to the leakage current of the detector and of the input Junction Field-Effect Transistor (JFET), is directly proportional to the shaping time. It was calculated based on the measured leakage current of the detector at different temperatures (Fig. 3) and on the estimated leakage current of the input JFET as a function of temperature.<sup>27</sup> The white series noise, due to the capacitance of the detector and of the input JFET, is inversely proportional to the shaping time. It was calculated based on the measured capacitance of the detector at different temperatures (Fig. 7) and on the estimated input capacitance of the input JFET of the preamplifier.<sup>27</sup> The  $1/f$  noise is shaping time-invariant. Although the dielectric noise and the charge trapping noise cannot be directly calculated, the difference between the total  $FWHM$  of the peak and the quadratic sum of the rest noise components (white series noise, white parallel noise,  $1/f$  noise, and Fano noise) were attributed to the quadratic sum of the dielectric and the charge trapping noise.

The  $FWHM$  increase, shown in Fig. 11, as the temperature increased was attributed to the white parallel noise and the quadratic sum of the dielectric and charge trapping noise increasing with temperature. The best energy resolution at 10 V reverse bias was achieved at short shaping times ( $\tau = 2 \mu\text{s}$ ) at 60 °C and 40 °C and at long shaping times ( $\tau = 10 \mu\text{s}$ ) at 20 °C and 0 °C. This was attributed to the fact that the parallel white noise increased with shaping time, the series white noise decreased with shaping time, and the quadratic sum of the dielectric and charge trapping noise was expected to be shaping time invariant. Hence, the energy resolution was found to be limited by the leakage current of the detector and/or the input JFET rather than their capacitances at  $T \geq 40^\circ\text{C}$ , whereas the opposite happened at  $T \leq 20^\circ\text{C}$ , over the investigated temperature range. To make this clearer, the total noise along with the calculated noise contributions at 60 °C and 10 V reverse bias is shown in Fig. 12 as a function of shaping time.

The dominant source of noise at shaping times up to  $5 \mu\text{s}$  was found to be the quadratic sum of the dielectric noise and charge trapping noise with a mean value of  $(775 \pm 30) \text{ eV}$ . However, the white parallel noise was the limiting factor for the energy resolution for  $\tau > 5 \mu\text{s}$ , at 60 °C and 10 V reverse bias. The parallel noise was found to be the dominant noise at long shaping times  $\tau > 5 \mu\text{s}$  for 5 V and 15 V reverse bias, whereas the sum of the dielectric noise and charge trapping noise was found to dominate at all shaping times, at 0 V and 60 °C. The dielectric noise, as a function of temperature, was estimated assuming that charge trapping noise at 15 V reverse bias was insignificant. This assumption was made due to the improved charge transport with increased reverse bias resulting in less trapping noise. The measured energy resolution at 15 V reverse bias and at each temperature was plotted as a function of shaping time and can be seen in Fig. 13. Following this, the  $FWHM$  was calculated based on the known noise sources (white series noise, white parallel noise,  $1/f$  noise, and Fano noise). Then, the difference between the total measured  $FWHM$  and the calculated noise including all the noise contributions discussed above was attributed to the dielectric noise. Since the dielectric noise was expected to be shaping time-invariant, the mean value and the rms error were



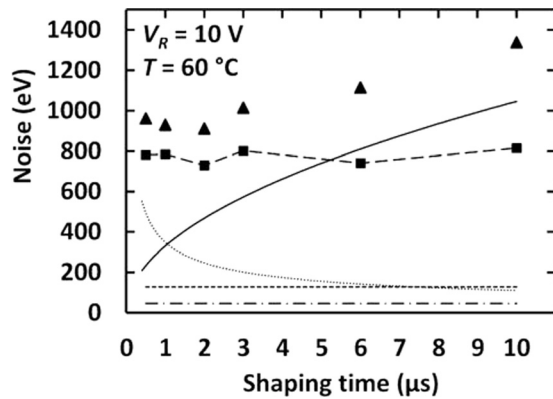


FIG. 12. Total measured  $FWHM$  of 5.9 keV peak (triangles) as a function of shaping time at 60 °C and 10 V reverse bias with the calculated noise components: quadratic sum of dielectric noise and charge trapping noise (squares), series white noise (round dots), parallel white noise (solid line), Fano noise (square dots), and  $1/f$  noise (long dash dot). Long dashes for the sum of dielectric and charge trapping noise are guides for the eyes only.

calculated for the dielectric noise as a function of shaping time at each temperature, at 15 V reverse bias. The total calculated  $FWHM$  at 5.9 keV, including the dielectric noise, can be seen in Fig. 13.

The estimated dielectric noise as a function of temperature can be seen in Fig. 14. It was found to increase from  $(716 \pm 29)$  eV at 0 °C to  $(872 \pm 74)$  eV at 60 °C. The larger uncertainty in the dielectric noise at 60 °C compared to lower temperatures was attributed to possible leakage current instabilities at high temperatures and 15 V reverse bias.

The measured  $FWHM$  of 5.9 keV at the temperature range 0 °C to 60 °C as a function of reverse bias can be seen in Fig. 15. The best energy resolution ( $FWHM$  at 5.9 keV) was achieved at 5 V reverse bias at each investigated temperature. It was measured to be 730 eV at 0 °C, 750 eV at 20 °C, 770 eV at 40 °C, and 840 eV at 60 °C. The other previously reported that 7  $\mu$ m GaAs devices had an energy resolution of  $\sim 1$  keV at room temperature<sup>14</sup> and thinner GaAs p-i-n mesa photodiodes (2  $\mu$ m) had  $\sim 1$  keV  $FWHM$  at 60 °C,<sup>12</sup> coupled to similar front-end electronics. The improving of the energy resolution was attributed to slightly lower electronic noise arising from the preamplifier in addition to better electrical characteristics (leakage current and capacitance) of the

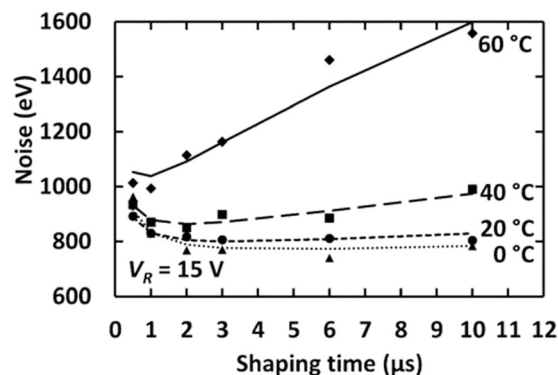


FIG. 13. Total measured (60 °C—diamonds; 40 °C—squares; 20 °C—circles; 0 °C—triangles) and calculated (60 °C—solid line; 40 °C—long dashes; 20 °C—square dots; 0 °C—round dots)  $FWHM$  of 5.9 keV peak as a function of shaping time at 15 V reverse bias.

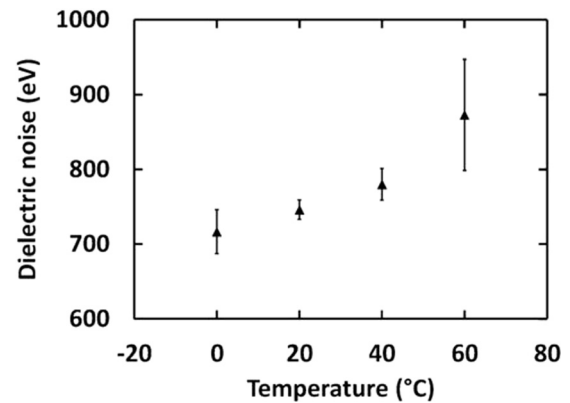


FIG. 14. Estimated dielectric noise as a function of temperature.

detector compared to those previously reported.<sup>12,14</sup> However, the best energy resolutions of Schottky GaAs detectors, which were coupled to ultra low noise front-end electronics (0.3 keV  $FWHM$  at 5.9 keV (Ref. 11)) and (0.266 keV  $FWHM$  at 5.9 keV (Ref. 10)), are far better than the currently reported mesa p-i-n device with ohmic contacts. The dominant source of noise in the system reported here, dielectric noise, has arisen from lossy dielectrics at the input of the preamplifier. These could be the packaging of the input JFET as well as the detector's package.

## VI. DISCUSSIONS, CONCLUSIONS, AND FUTURE WORK

Two randomly selected fully etched 200  $\mu$ m GaAs  $p^+-i-n^+$  mesa X-ray photodiodes have been electrically characterized within the temperature range 0 °C to 120 °C in addition to characterization of one of the diodes as detector for photon counting X-ray spectroscopy at the temperature range 0 °C to 60 °C. The ideality factor of the devices as a function of temperature was calculated based on the measured current as a function of applied forward bias. The ideality factor, which was found to improve from  $(1.94 \pm 0.01)$  at 0 °C for both devices to  $(1.78 \pm 0.03)$  and  $(1.79 \pm 0.05)$  at 120 °C for D1 and D2, respectively, indicated that the recombination current defined the forward current and its small temperature dependence excluded tunnelling from significant contribution to the forward current.

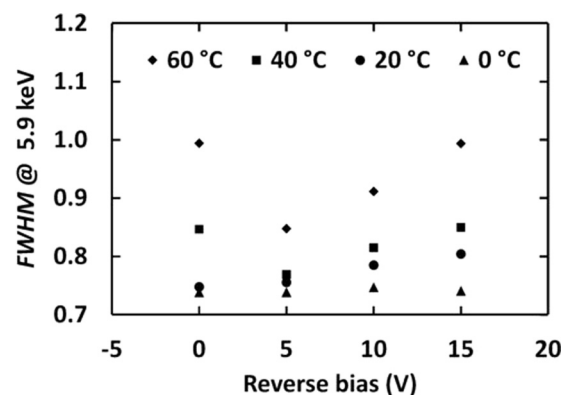


FIG. 15. Measured  $FWHM$  of 5.9 keV as a function of reverse bias at the temperature range 0 °C to 60 °C at  $\tau_{opt}$ .

The leakage current decreased with decreased temperature from  $(7.65 \pm 0.01) \times 10^{-9}$  A ( $24.36 \pm 0.05 \mu\text{A}/\text{cm}^{-2}$ ) at  $120^\circ\text{C}$  to  $(9 \pm 4) \times 10^{-13}$  A ( $3 \pm 1 \text{ nA}/\text{cm}^{-2}$ ) at  $0^\circ\text{C}$ , and from  $(2.950 \pm 0.007) \times 10^{-9}$  A ( $9.39 \pm 0.02 \mu\text{A}/\text{cm}^{-2}$ ) at  $120^\circ\text{C}$  to a current which was smaller than the uncertainty of the measurement,  $(0.8 \pm 4.0) \times 10^{-13}$  A ( $0.2 \pm 1.2 \text{ nA}/\text{cm}^{-2}$ ) at  $0^\circ\text{C}$  for D1 and D2, respectively, at 15 V reverse bias. The leakage current density of the devices found to exponentially increase with temperature with a constant factor, up to  $100^\circ\text{C}$ . However, the leakage current density at  $120^\circ\text{C}$  was found to be greater than the expected, for both devices. This was attributed to the diffusion current being the prevailing conduction process for temperatures higher than  $100^\circ\text{C}$ , in contrast to the generation current being dominant at lower temperatures.

The diffusion capacitance, at forward applied biases, decreased as the temperature decreased from  $120^\circ\text{C}$  to  $0^\circ\text{C}$ , due to the diffusion capacitance being directly proportional to the forward current. Measurements of the depletion layer capacitance as well as computation of the depletion layer width of the devices as a function of temperature suggested the presence of a thin region around the depletion layer with unionized dopants at low temperatures, which were progressively ionized with temperature. As a result, the depletion layer width was limited at high temperatures and low reverse biases from the ionized dopants, and a temperature dependent depletion layer capacitance was measured for reverse biases  $V_R \leq 1$  V. The i layer thickness was found to be  $(7.5 \pm 0.5) \mu\text{m}$  for D1 and  $(6.7 \pm 0.4) \mu\text{m}$  for D2. The carrier concentration was found to increase from  $(0.6 \pm 0.1) \times 10^{14} \text{ cm}^{-3}$  at  $5 \mu\text{m}$  below the  $p^+-i$  junction to  $(12.7 \pm 0.7) \times 10^{14} \text{ cm}^{-3}$  at the  $i-n^+$  interface for D1 and from  $(0.87 \pm 0.02) \times 10^{14} \text{ cm}^{-3}$  at  $5 \mu\text{m}$  below the  $p^+-i$  junction to  $(16 \pm 9) \times 10^{14} \text{ cm}^{-3}$  at the  $i-n^+$  interface for D2.

The X-ray detection performance of D1 was characterized as a function of temperature from  $0^\circ\text{C}$  to  $60^\circ\text{C}$ .  $^{55}\text{Fe}$  spectra were accumulated at different reverse bias conditions (0 V, 5 V, 10 V, and 15 V) and varied shaping time (0.5  $\mu\text{s}$ , 1  $\mu\text{s}$ , 2  $\mu\text{s}$ , 3  $\mu\text{s}$ , 6  $\mu\text{s}$ , and 10  $\mu\text{s}$ ). The lowest *FWHM* at each temperature was measured at 5 V reverse bias: 730 eV at  $0^\circ\text{C}$ , 750 eV at  $20^\circ\text{C}$ , 770 eV at  $40^\circ\text{C}$ , 840 eV at  $60^\circ\text{C}$ . The *FWHM* increase with temperature was attributed to the white parallel noise and the quadratic sum of the dielectric and charge trapping noise increase as the temperature increased. Subsequent noise analysis at  $60^\circ\text{C}$  revealed that the sum of the dielectric and charge trapping noise was the dominant source of noise at all shaping times at 0 V reverse bias and at short shaping time ( $\tau \leq 5 \mu\text{s}$ ) at high reverse biases (5 V, 10 V, and 15 V), whereas the white parallel noise was the main source of noise at long shaping times ( $\tau > 5 \mu\text{s}$ ) at high reverse biases.

An estimation of the dielectric noise, arising from lossy dielectrics at the input of the preamplifier, at each temperature was feasible assuming the charge trapping noise at 15 V was negligible. It was found to increase from  $(716 \pm 29)$  eV at  $0^\circ\text{C}$  to  $(872 \pm 74)$  eV at  $60^\circ\text{C}$ . Although the energy resolution (*FWHM* at 5.9 keV) of the GaAs  $p^+-i-n^+$  mesa photodiodes reported here is better than previously reported similar and thinner mesa X-ray photodiodes (1 keV *FWHM* at

5.9 keV at room temperature<sup>14</sup> and 1 keV *FWHM* at 5.9 keV at  $60^\circ\text{C}$ ,<sup>12</sup> respectively), it is far from the best experimental reports, with GaAs planar  $p-i-n$  diodes with Schottky contacts and guard rings at room temperature (0.3 keV (Ref. 11) and 0.266 keV (Ref. 10) *FWHM* at 5.9 keV) when operated with ultra low noise front end electronics. The elimination of the parasitic dielectric noise could lead to the improvement of the energy resolution of the currently reported system and is part of the future work through novel redesign of the pre-amplifier input.

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